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EXAMINER	
RAMPURIA, SATISH	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/910,206	BEUTEN ET AL.	
	Examiner	Art Unit	
	SATISH RAMPURIA	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date. _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Amendment

1. This action is in response to the RCE received on 12/08/2008.

2. New claims added by the applicants: 15-17.

3. Claims 1-14 are pending.

Continued Examination Under 37 CFR 1.114

4. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/08/2008 has been entered.

Response to Arguments

5. Applicant's arguments filed 11/14/2007 have been fully considered but they are not persuasive.

In the remarks, the applicant has argued that:

Therefore, Ross does not identically disclose (or even suggest) all of the features of claim 1, including the features *of causing the debug logic to trigger an exception* upon access to a specific address range during a program execution time, and *causing the debug logic to execute an exception routine* after the exception is triggered during the program execution time, in which *the access to the specific address range includes access to an illegal storage area,* in which *the debug logic and its registers are operated in parallel to the program execution time..., so as to provide a secure stack check without using the program execution time of the microprocessor,* and in which *the debug logic monitors a program run.* See page 10.

Examiner's response:

In response to Applicants arguments, Ross's system discloses a debug facility to provide information to a system or application program of another program's access to shared resources and allow the computer system to perform a notification. More particularly, Ross discloses in figures 3, 5A and 5B that the system shows the application program of a peripheral device accessing an address which causes the breakpoint to trigger (col. 4, lines 37-56) i.e., causing the debug logic to trigger an exception upon access to an address. Then the callback routing is executed that indicates the stored breakpoint is accessed via another program (col. 4, lines 37-56), i.e., executing an exceptional routine after the exception is triggered. Further, Ross discloses that a specified address in being accessed by another program which causes an interrupt at the determined address (col. 5, lines 7-15) i.e., accessing to an illegal storage area or protected address.

Furthermore, Ross discloses that once the breakpoint is accessed by the another program, e.g., program 1. The system of Ross transfers to a monitor mode, and the breakpoint register is monitored by processor to determine whether the breakpoint has been triggered as indicated in the specified address (col. 4, lines 57-66) i.e., monitoring of the program 1 and program 2 are operating in parallel, in addition, an example as described by Ross that

program 1 (electronic mail) and program 2 (monitor power down) are operating in parallel (col. 5, lines 32-47).

Finally, Ross discloses the register is accessed to determine the address which caused the interrupt co 3 lines 65 to col. 4 line 2, specifically at col. 5 lines 6-12 and the interrupt handler routine then continues executing (col. 5, lines 25-27). Note that the secure stack check is inherently done without using the program execution time of the microprocessor when the debug logic and its register are operated in parallel to the program execution time. Therefore, the rejection is proper and maintained herein.

With respect to claim 9, rejection clearly points out where Ross and Rowland disclose the cited limitations and why it would have been obvious to one skill in the art. Rowland clearly discloses swapping the memories with having the new executable code burned in as claimed, see the rejection below. The motivation to swap the memories to read and write newer data control relationship during engine operations, see the rejection below.

With respect to claim 12, rejection clearly points out where Ross and APA disclose the cited limitations and why it would have been obvious to one skill in the art. APA clearly indicates that a type of micro controller is used in motor vehicle as claimed in claim 12, see the rejection below. The motivation to have a microcontroller in motor vehicle to control the various parts of the motor vehicle such as control of the internal combustion engine, the

transmission, the steering assembly, the chassis, etc. as taught by APA. Accordingly, the rejection to claim 12 is maintained herein.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-8, 10-11, 13-14 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,680,620 to Ross hereinafter called Ross.

Per claim 1:

Ross discloses:

A program stored in a computer readable medium, the program performing a method for monitoring an execution of another program that is executable on at least one microprocessor of a micro controller using a debug logic of the micro controller (abstract, "in a microprocessor, a debug facility traps access to a peripheral device.), comprising:

- *causing the debug logic to trigger an exception upon access to an specific address range during a program execution time* (col. 3 line 65 to col. 4 line 2 "application program specifies a breakpoint in the debug register circuit 13. The breakpoint is a trap or software exception

that is triggered when a specified I/O or memory address accessed" and col. 4 liens 9-11, "Debug registers DR0-DR4 can each hold an I/O or memory address as a breakpoint (an specific address range));

- *causing the at least one microprocessor to configure the debug logic* (col. 4 lines 10-13, "the condition for generating a debug exception in the Pentium microprocessor is specified in the Debug Control Register."), and

- *causing the debug logic to execute an exception routine after the exception is triggered during the program execution time* (col. 3 line 65 to col. 4 line 2 "application program specifies a breakpoint in the debug register circuit 13. The breakpoint is a trap or software exception that is triggered when a specified I/O or memory address accessed);

- *wherein the access to the specific address range includes access to an illegal storage area* (col. 3 line 65 to col. 4 line 2 "application program specifies a breakpoint in the debug register circuit 13. The breakpoint is a trap or software exception that is triggered when a specified I/O or memory address accessed");

- *wherein the debug logic and its registers* (program 2) *are operated in parallel to the program execution time* (col. 5 lines 33-35, program 2 is another program such as a monitor power down program which is operating in parallel with program 1) *to check a stack having the specific address range and an exception routine is set up in reaction to a break point event in the stack, so as to provide an secure stack check without using the program*

execution time of the microprocessor, wherein the debug logic monitors a program run (co 3 line 65 to col. 4 line 2, specifically at col. 5 lines 6-12, "the register is accessed to determine the address which caused the interrupt.", col. 5, lines 25-27, "the interrupt handler routine then continues executing.", Note that the secure stack check is inherently done without using the program execution time of the microprocessor when the debug logic and its register are operated in parallel to the program execution time);
wherein the debug logic monitors a program run (col. 4, lines 44-46 "This address is provided by the program desiring the monitoring, e.g., program 2 in FIG. 5A").

Per claim 2:

The rejection of claim 1 is incorporated and further, Ross discloses:
wherein: the exception corresponds to an interrupt of the execution of the program (col. 3 line 65 to col. 4 line 2 "application program specifies a breakpoint in the debug register circuit 13. The breakpoint is a trap or software exception that is triggered when a specified I/O or memory address accessed").

Per claim 3:

The rejection of claim 1 is incorporated and further, Ross discloses:

wherein: the debug logic is configured during a startup of the micro controller (col. 3 line 65 to col. 4 line 2 "application program specifies a breakpoint in the debug register circuit 13. The breakpoint is a trap or software exception that is triggered when a specified I/O or memory address accessed". Note that the startup of the micro controller is inherently done without startup of microcontroller the breakpoint cannot be specified).

Per claim 4:

The rejection of claim 1 is incorporated, and further, Ross discloses:
resetting the micro controller, starting up the micro controller again, and initializing the program (col. 4, lines 57-62 "After the system is initialized, the system transfers to a monitor mode of operation. During the monitor mode, as indicated by monitor step 108, the breakpoint register is monitored by processor 12 to determine whether the breakpoint has been triggered, as indicated by the address location which is held as the breakpoint value being accessed").

Per claim 5:

The rejection of claim 4 is incorporated, and further, Ross discloses:
storing at least a type of a fault in a memory storing at least a type of a fault in a fault memory before the micro controller is reset and started up again and before the program is

initialized (col. 4, lines 50-53 "at callback address step 104, the callback address of the routine to be called is stored within debug (fault) table 106 within memory 36". Note that in computer environment faults are called 'bugs').

Per claim 6:

The rejection of claim 1 is incorporated, and further, Ross discloses:

storing a memory address that was accessed before an occurrence of the fault in the fault memory before the micro controller is reset and started up again and before the program is initialized (col. 4, lines 50-53 "at callback address step 104, the callback address of the routine to be called is stored within debug (fault) table 106 within memory 36". Note that in computer environment faults are called 'bugs').

Per claim 7:

The rejection of claim 1 is incorporated, and further, Ross discloses:

the debug logic monitors whether the program accesses a preselectable address range of a memory during the program execution time (col. 3 line 65 to col. 4 line 2 "application program specifies a breakpoint in the debug register circuit 13. The breakpoint is a trap or software exception that is triggered when a specified I/O or memory address accessed").

Per claim 8:

The rejection of claim 7 is incorporated, and further, Ross discloses:

wherein: the debug logic monitors whether the program accesses an address range of a stack of the micro controller beyond a preselectable maximum stack size during the program execution time (col. 3 line 65 to col. 4 line 2 "application program specifies a breakpoint in the debug register circuit 13. The breakpoint is a trap or software exception that is triggered when a specified I/O or memory address accessed").

Claim 10 is the apparatus (micro controller) claim corresponding to computer readable medium claim 1, and rejected under the same rational set forth in connection with the rejection of claim 1, above, as noted above.

Per claim 11:

The rejection of claim 10 is incorporated, and further, Ross discloses:

the control element corresponds to one of a read-only memory and a flash memory (col. 3 lines 19-21 "Nonvolatile memory 38 is e.g. a read only memory (ROM) which stores microcode including the basic input output system").

Claims 13 and 14 are the apparatus (micro controller) claim corresponding to computer readable medium claims 1 and 2 respectively, and rejected under the same rational set forth in connection with the rejection of claims 1 and 2 respectively, above, as noted above.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a)A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 9, 15-17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ross in view of US Patent No. 6,535,811 to Rowland et al., hereinafter called Rowland.

Per claim 9:

Ross does not explicitly disclose a code sequence of the program, swapped out from a flash memory of the micro controller into a random access memory of the micro controller, in the flash memory.

However, Rowland discloses in an analogous computer system a code sequence of the program, swapped out from a flash memory of the micro controller into a random access memory of the micro controller, in the flash memory (col. 5, lines 23-25 “memory holding

the executable code, typically some type of ROM, had to be swapped with a memory having the new executable code "burned in."" and col. 5, lines 27-29 “flash memory 22 comprises a flash EPROM. Thus, executable code for the microcontroller can be rewritten as necessary”).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of swapping the code between memories as taught by Rowland into the method of monitoring the program as taught by Ross. The modification would be obvious because of one of ordinary skill in the art would be motivated to swap the code between flash and RAM memories to read write the data control relationship during engine operation as suggested by Rowland (col. 2, lines 5-9).

Per claims 15 and 17:

The rejection of claims 13 and 10 respectively, incorporated and further Ross discloses:

a memory address is stored that was accessed before an occurrence of the fault in the fault memory and at least a type of a fault is stored in a fault memory, before the micro controller is reset and started up again and before the program is initialized (col. 4, lines 50-53 “at callback address step 104, the callback address of the routine to be called is stored within debug (fault) table 106 within memory 36”. Note that in computer environment faults are called ‘bugs’),

during the execution of the exception routine, the micro controller is reset, the micro controller is started up again, and the program is initialized (col. 4, lines 57-62 “After the system is initialized, the system transfers to a monitor mode of operation. During the monitor mode, as indicated by monitor step 108, the breakpoint register is monitored by processor 12 to determine whether the breakpoint has been triggered, as indicated by the address location which is held as the breakpoint value being accessed”),

the exception corresponds to an interrupt of the execution of the program (col. 3 line 65 to col. 4 line 2 "application program specifies a breakpoint in the debug register circuit 13. The breakpoint is a trap or software exception that is triggered when a specified I/O or memory address accessed”),

the debug logic is configured during a startup of the micro controller (col. 3 line 65 to col. 4 line 2 "application program specifies a breakpoint in the debug register circuit 13. The breakpoint is a trap or software exception that is triggered when a specified I/O or memory address accessed". Note that the startup of the micro controller is inherently done without startup of microcontroller the breakpoint cannot be specified),

the debug logic monitors whether the program one of (i) accesses a preselectable address range of a memory during the program execution time (col. 3 line 65 to col. 4 line 2 "application program specifies a breakpoint in the debug register circuit 13. The breakpoint is a trap or software exception that is triggered when a specified I/O or memory address

accessed"), and (ii) accesses an address range of a stack of the micro controller beyond a preselectable maximum stack size during the program execution time (col. 2, lines 34 "generating a device access interrupt when the address is accessed" and col. 4, lines 50-52 "callback address… is stored within debug table 106 within memory")(debug table here is interpreted as stack in the memory), and

Ross discloses the debug logic monitors whether an attempt is made during the program execution time to execute a code sequence of the program in a first type of memory (col. 2, lines 33 "monitoring the breakpoint within the debug circuit to determine whether the address is accessed" Here address is accessed from the memory). Ross does not explicitly disclose swapping the first type of memory of the micro controller into another type of memory of the microcontroller.

However, Rowland discloses in an analogous computer system swapping the first type of memory of the micro controller into another type of memory of the microcontroller (col. 5, lines 23-25 "memory holding the executable code, typically some type of ROM, had to be swapped with a memory having the new executable code "burned in."" and col. 5, lines 27-29 "flash memory 22 comprises a flash EPROM. Thus, executable code for the microcontroller can be rewritten as necessary").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of swapping the code between memories as taught by Rowland into the method of monitoring the program as taught by Ross. The modification would be obvious because of one of ordinary skill in the art would be motivated to swap the code between flash and RAM memories to read write the data control relationship during engine operation as suggested by Rowland (col. 2, lines 5-9).

Claim 16 is the computer readable claim corresponding to apparatus claim 15, and rejected under the same rational set forth in connection with the rejection of claim 1, above, as noted above.

10. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ross in view of Admitted Prior Art, hereinafter called APA.

Per claim 12:

The rejection of claim 10 is incorporated, and further, Ross does not explicitly disclose the micro controller is arranged in a motor vehicle.

However, APA discloses in an analogous computer system the micro controller is arranged in a motor vehicle (Applicant's specification, page 2, lines 4-5 "This type of micro controller is, for example, part of a controller for a motor vehicle").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of the micro controller is arranged in a motor vehicle as taught by APA into the method of monitoring the program as taught by Ross. The modification would be obvious because of one of ordinary skill in the art would be motivated to have the micro controller is arranged in a motor vehicle to provide the control of the internal combustion engine, the transmission, the steering assembly, the chassis, etc. as suggested by APA (page 2, lines 1-10).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Satish S. Rampuria** whose telephone number is **(571) 272-3732**. The examiner can normally be reached on **8:30 am to 5:00 pm** Monday to Friday. Any inquiry of a general nature or relating to the status of this application should be directed to the **TC 2100 Group receptionist: 571-272-2100**

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Wei Y. Zhen** can be reached on **(571) 272-3708**. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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